We claim:

1. A method for processing data using a programmable processor comprising:

decoding a single instruction for writing data to memory specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register;

detecting some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and

writing the write-enabled data fields to a specified memory location.

2. The method of claim 1 wherein each of the fields of the mask has a width of one bit.

3. The method of claim 1 wherein each of the fields of the data contained in the register has a width of one bit.

4. The method of claim 1 wherein the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location.

5. The method of claim 1 wherein the mask is contained in a specified register.

6. The method of claim 1 wherein the memory location is contained in a specified register.

7. The method of claim 1 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

8. The method of claim 1 wherein the predetermined value is a logic 1.

9. The method of claim 1 further comprising:

decoding a second single instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products; and

providing the plurality of products to partitioned fields of a result register as a catenated result.

10. A computer-readable medium:

having instructions that instruct a computer system to perform operations,

at least some of the instructions including a store multiplex instruction for selectively storing data in a programmable processor, the store multiplex instruction capable of instructing a computer to perform operations comprising:

decoding the store multiplex instruction specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register;

detecting some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and

writing the write-enabled data fields to a specified memory location.

11. The computer-readable medium of claim 10 wherein each of the fields of the mask has a width of one bit.

12. The computer-readable medium of claim 10 wherein each of the fields of the data contained in the register has a width of one bit.

13. The computer-readable medium of claim 10 wherein the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location.

14. The computer-readable medium of claim 10 wherein the mask is contained in a specified register.

15. The computer-readable medium of claim 10 wherein the memory location is contained in a specified register.

16. The computer-readable medium of claim 10 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

17. The computer-readable medium of claim 10 wherein the predetermined value is a logic 1.

18. The computer-readable medium of claim 10 wherein at least some of the instructions further include a group floating point multiply instruction for multiplying floating point data in a programmable processor, the group floating point multiply instruction capable of instructing the computer to perform operations comprising:

decoding the group floating point multiply instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products; and

providing the plurality of products to partitioned fields of a result register as a catenated result.

19. A computer data signal, embodied in a transmission medium:

having instructions that instruct a computer system to perform operations,

at least some of the instructions including a store multiplex instruction for selectively storing data in a programmable processor, the store multiplex instruction capable of instructing a computer to perform operations comprising:

decoding the store multiplex instruction specifying both a mask and a register containing data, the mask comprising fields that each correspond to a field of the data contained in the register;

detecting some of the fields of the mask as having a predetermined value and identifying corresponding fields of the data contained in the register as write-enabled data fields; and

writing the write-enabled data fields to a specified memory location.

20. The computer data signal of claim 19 wherein each of the fields of the mask has a width of one bit.

21. The computer data signal of claim 19 wherein each of the fields of the data contained in the register has a width of one bit.

22. The computer data signal of claim 19 wherein the writing step further comprises reading an unaltered field of data from the specified memory location and writing the unaltered field of data along with the write-enabled data fields to the specified memory location.

23. The computer data signal of claim 19 wherein the mask is contained in a specified register.

24. The computer data signal of claim 19 wherein the memory location is contained in a specified register.

25. The computer data signal of claim 19 wherein the specified memory location comprises a section of memory having a specific width and beginning at a specific memory address.

26. The computer data signal of claim 19 wherein the predetermined value is a logic 1.

27. The computer data signal of claim 19 wherein at least some of the instructions further include a group floating point multiply instruction for multiplying floating point data in a programmable processor, the group floating point multiply instruction capable of instructing the computer to perform operations comprising:

decoding the group floating point multiply instruction specifying a third and a fourth register each containing a plurality of floating-point operands;

multiplying the plurality of floating point operands in the third register by the plurality of operands in the fourth register to produce a plurality or products; and

providing the plurality of products to partitioned fields of a result register as a catenated result.